a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

20 ~~36~~. (Twice Amended) An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, disposed between a first power supply and a second power supply, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit, coupled to the differential amplifier circuit and the first and second circuits, for selectively enabling the differential amplifier circuit and one of the first circuit and the second circuit in accordance with a control signal while isolating the other one of the first circuit and the second circuit from the first power supply or the second power supply.

25~~43~~. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit in accordance with the control signal.

26~~44~~. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

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27~~45~~. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

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46. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating a single amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

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Cont

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal and generating a single output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit in accordance with the control signal.

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47. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating a single amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

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